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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Noriaki Sakamoto et al.
Serial No. : 09/810,105
Filed : March 16, 2001
Title : SEMICONDUCTOR DEVICE

Art Unit : 2811
Examiner : Parekh, Nitin

#7

Response
J. McClellan
10/16/02

BOX AF
Commissioner for Patents
Washington, D.C. 20231

REMARKS

Applicants respond to the action mailed July 3, 2002 as follows:

Claims 1 to 3 and 5 to 16 have been rejected as being unpatentable over Fukutomi et al. in view of Fjelstad and Kweon et al. No claims have been amended in this response. Applicants submit that the cited claims are unobvious for the following reasons.

Claim 1 recites as follows:

> 1. (Twice Amended) A semiconductor device comprising:
> a plurality of conductive paths electrically separated from one another by a trench;
> a first conductive path of said plurality of conductive paths, having a die pad shape;
> a semiconductor chip disposed over said first conductive path; **said first conductive path coupled to said semiconductor chip through a thermally conductive material**;
> a second conductive path disposed peripherally around said semiconductor chip, having a bonding pad shape;
> a third conductive path having a shape of an external connecting pad and coupled to said second conductive path, **said third conductive path being disposed underneath said semiconductor chip and coupled to said semiconductor chip through an insulating material**;
> connecting means for electrically connecting said semiconductor chip to said second conductive path;

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insulating resin covering said semiconductor chip, filling in the trench, and integrally supporting the semiconductor chip and the conducive paths with a bottom surface of the paths exposed. (Emphasis added.)

The above bolded features, which were stressed in the previous response, were not addressed in the Final office action. To reiterate, Fukutomi et al. in view of Fjelstad and Kweon et al. does not show a structure as claimed in claim 1 where the first conductive path, which is disposed underneath the semiconductor chip, is coupled to the semiconductor chip through a thermally conductive material, and the third conductive path, also disposed underneath the semiconductor chip, is coupled to the semiconductor chip through an insulating material.

Fukutomi et al. shows a die-bonding material 66 bonding the chip 65 to the wiring patterns 63 (see Fig. 22c). Fjelstad shows gold being selectively plated to the first surface 401 and bonded to the entire undersurface of the chip 420 (see Fig. 7D and column 8, lines 13 to 17). Kweon et al. shows an Ag-epoxy adhesive 120 dispose below the entire surface of the chip 110 (see Fig. 10). A combination of the cited prior art does not disclose, teach, or suggest a configuration as claimed in claim 1. That is, none of the cited references show two different conductive paths underneath the semiconductor chip with **one path coupled to the chip through a thermally conductive material and another path coupled to the chip through an insulating material**. Thus, a person of ordinary skill in the art would not have found obvious the present invention of claim 1 by the combination of the cited prior art.

Claims 2, 3, 5 to 13 depend on claim 1 directly or indirectly. Therefore, these clams are also unobvious at least for the same reason as claim 1.

Claim 14 recites:

14. (Amended) A semiconductor device comprising:
a plurality of conductive paths electrically separated from one another by a trench;
a semiconductor chip connected with at least one of said conductive paths through a thermal conductive material; and
insulating resin which covers said semiconductor chip, is embedded in the trench among said plurality of conductive paths and integrally supports the conducive paths, rear surface of which are at least partially exposed from the insulating resin.

wherein at least another one of said conductive paths is disposed at a periphery of said semiconductor chip and extends underneath the chip and coupled to the chip through an insulating material to form an external terminal. (Emphasis added.)

Because claim 14 has similar limitations as claim1, claim14 would not have been obvious to a person of ordinary skill in the art at least for the same reason as claim 1.

Claims 15 and 16, which depend on claim 14, are also unobvious at least for the same reason as claim 14.

Furthermore, claim 12 is also not taught or suggested by the cited references. Claim 12 recites:

12. (Amended) A semiconductor device according to claim 1, wherein said first conductive path is coupled with a conductive pattern formed on a mounting board through a thermally conductive material.

This together with claim 1 states that the device has the following layered configuration: the semiconductor chip--thermally conductive material--the first conductive path--thermally conductive material-the conductive pattern. This configuration is not taught or suggested by any of cited prior art references.

Attached is a marked-up version of the changes being made by the current amendment.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 10/3/02

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